

REMARKS

This application contains claims 1-50. Claims 2, 3, 28 and 29 have been canceled without prejudice. Claims 1 and 27 are hereby amended. No new matter has been introduced. Reconsideration is respectfully requested.

Claims 1-3, 5, 11, 12, 21-29, 31, 37, 38 and 47-50 were rejected under 35 U.S.C. 102(b) over Gaddis et al. (U.S. Patent 5,815,501). Applicant has amended independent claims 1 and 27 in order to clarify the distinction of the present invention over the cited art. Amended claim 1 incorporates the limitations of original claims 2 and 3, while amended claim 27 incorporates the limitations of original claims 28 and 29.

Gaddis describes an ATM-Ethernet portal and concentrator, which is said to permit transparent interconnection between Ethernet segments over an ATM network (abstract). Gaddis shows in Fig. 9 how ATM cells are transferred from an ATM cell processor into shared memory, reassembled, and then transmitted onto an Ethernet segment. The ATM cell processor places the cells in the shared memory in the order in which they arrive. This figure assumes that cells arrive in order (col. 10, lines 1-5).

Fig. 10 in Gaddis, on the other hand, shows the general case in which cells do not arrive in order (col. 10, lines 46-50). It can be seen in the figure that in this case, for example, CELL 2 of FRAME 1 is written to the memory before CELL 1 of FRAME 1. The Ethernet controller must assemble the frame from the non-contiguous locations of the segments based on a transmit buffer descriptor list that it receives from the control microprocessor in the portal (col. 10, lines 35-40).

Claim 1, as amended, recites a network interface device, which receives a sequence of data packets from a network. A protocol processor processes the headers of the packets in order to identify a group of packets that contain fragments of a data frame. The fragments have a fragment order, which may be different from the sequence in which the data packets were received. The protocol processor controls host interface logic, however, so that the logic allocates space for the data frame in host memory and reassembles the fragments in the allocated memory space

in the fragment order, regardless of whether the packet sequence coincides with the fragment order. This approach is advantageous in that it enables the host processor to access the frame payload data immediately when the entire frame has been received, without the processing burden of frame reassembly (see page 5, lines 2-11, in the present patent application).

Gaddis explicitly shows in Fig. 10 that even when ATM cells arrive out of order with respect to the Ethernet frame whose segments they are carrying, the cells are written to memory in their order of arrival. In other words, to paraphrase the terminology of claim 1, the portal writes the cells to the memory in the sequence in which they arrive, regardless of whether this sequence coincides with the segment order. Gaddis neither teaches nor suggests that his portal might reassemble the ATM cells in memory according to the segment order when the segment order differs from the cell arrival sequence. He therefore cannot be taken to anticipate the fragment-order reassembly performed by the host interface logic of claim 1.

Thus, claim 1 as amended is believed to be patentable over Gaddis. In view of the patentability of claim 1, dependent claims 5, 11, 12 and 21-26 are believed to be patentable, as well.

Independent claim 27 recites a method for interfacing a host processor to a network, which operates on principles similar to the device of claim 1. Claim 27 has been amended in like manner to claim 1, and is therefore believed to be patentable for the reasons stated above. In view of the patentability of claim 27, dependent claims 31, 37, 38 and 47-50 are also believed to be patentable.

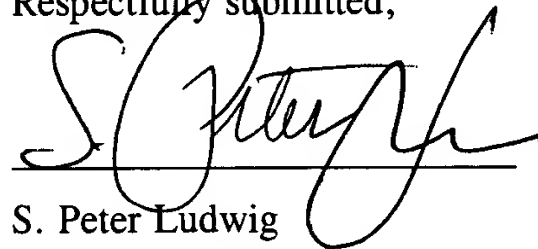
Claims 4, 6-10, 13-20, 30, 32-36 and 39-46 were rejected under 35 U.S.C. 103(a) over Gaddis in combination with one or more of Cowger et al. (U.S. Patent 6,314,477), Sandorfi et al. (U.S. Patent 5,590,122), Unekawa (U.S. Patent 5,706,425), Munger et al. (U.S. Patent 6,502,135), Ding (U.S. Patent 5,699,361) and Derango et al. (U.S. Patent 6,137,796). These claims all depend, directly or indirectly, from one of independent claims 1 and 27. In view of the patentability of the amended independent claims, as explained above, dependent claims 4, 6-10, 13-20, 30, 32-36 and 39-46 are also believed to be patentable.

Applicant has studied the additional references that were made of record by the Examiner. Applicant believes that all the claims in the present patent application are patentable over these additional references, whether the references are taken individually or in combination.

Applicant believes the amendments and remarks presented hereinabove to be fully responsive to all of the grounds of rejection raised by the Examiner. In view of these amendments and remarks, Applicant respectfully submits that all of the claims in the present application are in order for allowance. Notice to this effect is hereby requested.

Date: April 20, 2005

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'S. Peter Ludwig', is written over a horizontal line.

S. Peter Ludwig

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